SYNOPSYS®

DATASHEET

IC Validator Physical Verification

High-performance physical verification solution delivers up to 2X faster physical signoff

Overview

Synopsys' IC Validator physical verification is a comprehensive signoff solution improving productivity for customers at all process nodes from mature to advanced. The IC Validator tool offers the industry's best distributed processing scalability to over 2000 CPU cores. The tool's performance and scalability has enabled some of the industry's largest reticle limit chips with billions of transistors, same day design rule checking (DRC), layout versus schematic (LVS), and dummy fill turnaround time.

IC Validator physical verification is seamlessly integrated with Fusion Compiler™ RTL-to-GDSII solution and IC Compiler® II place and route system in the Fusion Design Platform. This integrated physical verification Fusion Technology™ accelerates design closure for manufacturing by enabling independent signoff-quality analysis and automatic repair within the implementation environment.

Benefits

- Industry leading physical verification performance enabled by distributed processing scalability past 2000 CPU cores
- Cloud-ready physical signoff, certified by TSMC
- Explorer technology for 5X faster DRC verification during SoC integration
- Elastic CPU management adds and removes CPUs dynamically
- Physical Verification Fusion within place and route enabling automatic DRC repair, timing aware FILL, and engineering change order (ECO) capabilities
- LVS-aware simulation based short-finder
- Integration with StarRC™ parasitic extraction, Custom Compiler™ full-custom design environment, and other third-party layout tools for increased designer productivity
- Live DRC for signoff quality on-the-fly DRC checking within full custom layout design tools
- Programmable Electrical Rule Checks (PERC) for customized checking for EOS/ESD/ERC rules
- Signoff certified at leading foundries with the broadest qualification and runset availability

Leading Performance and Scalability

IC Validator is architected for massively parallel distributed processing. IC Validator enables excellent scalability to 2000+ CPU cores. The built-in memory awareness keeps jobs within machine memory resource limits. IC Validator's elastic CPU management adds and removes CPUs dynamically. Intelligent file management balances disk, memory and speed up multi-host environment.

IC Validator is a cloud ready physical signoff solution. Its secure, scalable and certified by TSMC for signoff.

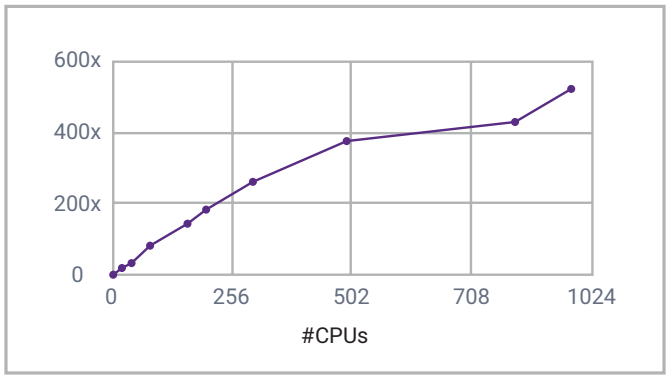

Figure 1: IC Validator scalability

IC Validator's smart load sharing technology continuously monitors jobs and determines job health. Jobs that crash are restarted on other CPU cores. CPU cores can be added or removed on the fly allowing the job to smartly adjust according to job needs and farm constraints. Memory aware scheduling estimates memory requirements in advance and schedules jobs based upon hardware configurations allotted for any given run. This means that physical verification jobs always run as efficiently as possible even on highly restrictive and heavily loaded compute farms. This is essential considering hundreds or even thousands of CPUs are required for today's modern chips.

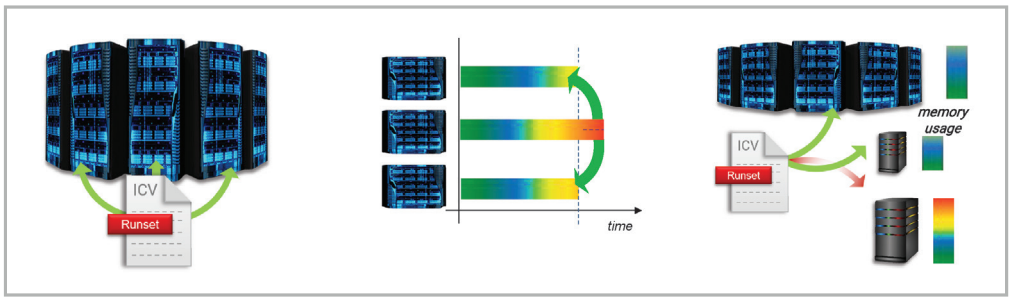

Figure 2: : Intelligent job management

Elastic CPU Management for distributed run provides designers with complete control over runtime expectations. There is no requirement to wait for all CPU's to become available before the job is launched. For example, if the job requires 128 CPUs and only 16 are available, the IC Validator job can be launched immediately with available CPUs. More CPUs can be added dynamically during the run, as CPUs become available. This enables designers to start the jobs early and finish the job early. Users also can add more CPUs to the job during peak to reduce the runtime. As the run progresses, you can use the remove_host capability to reduce your CPU usage freeing up valuable farm resources.

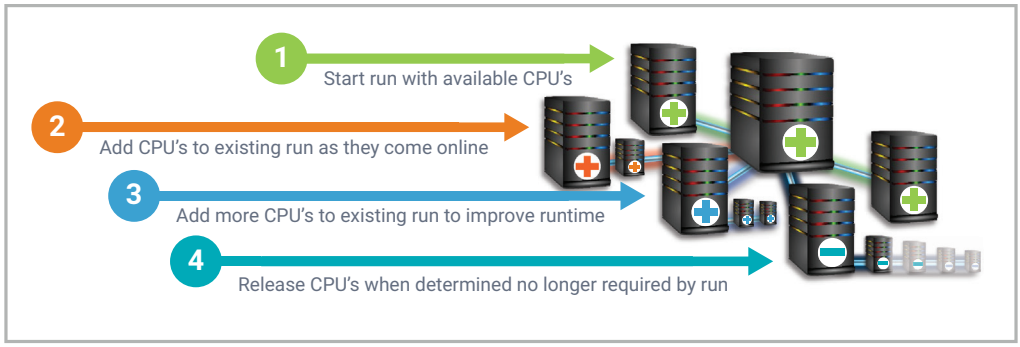

Figure 3: Elastic CPU management

Explorer DRC

IC Validator's innovative Explorer DRC technology is a paradigm shift in how very big, very dirt designs are handled from the early SoC integration stages, to final full chip DRC signoff. For design verification during SoC integration, Explorer DRC offers 5X faster runtime with 5X fewer CPUs. Additionally, Heatmap based debugging enables order-of-magnitude debugging speedup.

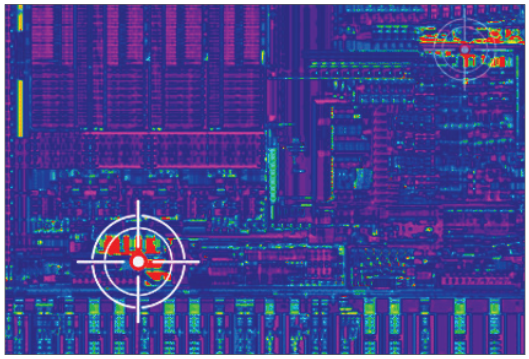

Figure 4: Explorer DRC identifies dense DRC error locations quickly

In early stages of full chip integration, a design can typically have 10's of billions of DRC errors. Gross design weaknesses such as incorrect block placement, fill overlap should be the initial focus. Incorrectly rotated blocks or block overlaps can lead to billions of DRC violations that can be less than obvious to designers. Days can be wasted re-running DRC before designers identify fundamental design flaws.

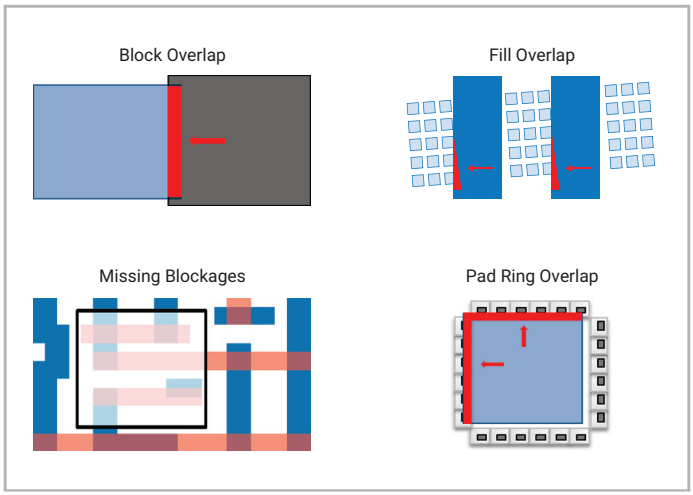

Figure 5: Examples of design weaknesses during SoC integration

Heatmap debugging with Explorer DRC allows designers to debug billions of DRC violations very quickly. Users are shown either in supported layout environments or directly in IC Validator - Visualization User Environment (VUE) heatmap details that enable designers to quickly pinpoint fundamental design flaws. DRC Heatmap provides designers with DRC error type, error density, error location, and error congestion.

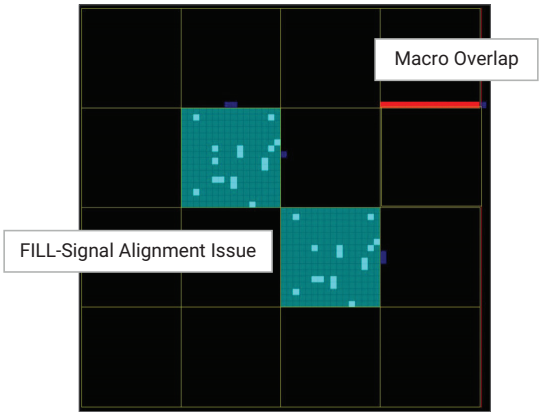

Figure 6: DRC heatmap highlighting error locations, density, and severity

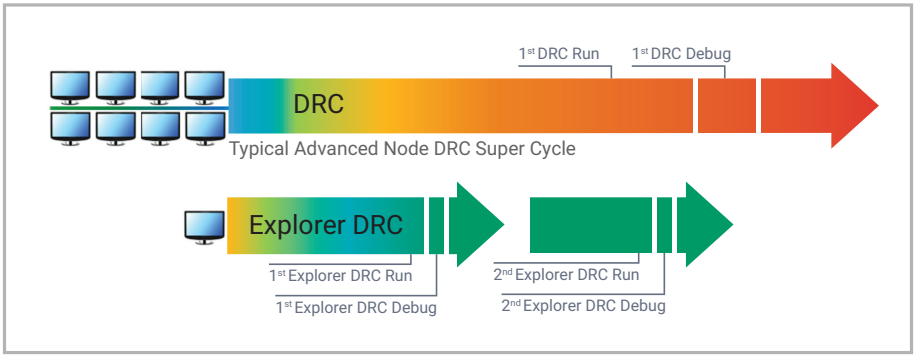

Figure 7: Explorer DRC accelerates physical signoff TAT

Physical Verification Fusion Technology

IC Validator brings the power of full signoff physical verification into the design phase with IC Compiler II, without imposing time-consuming stream-in and stream-out of layout data. Using physical verification Fusion, DRC and manufacturing issues are caught much earlier in the design cycle, reducing or eliminating late-stage surprises close to tapeout.

Automatic DRC Repair

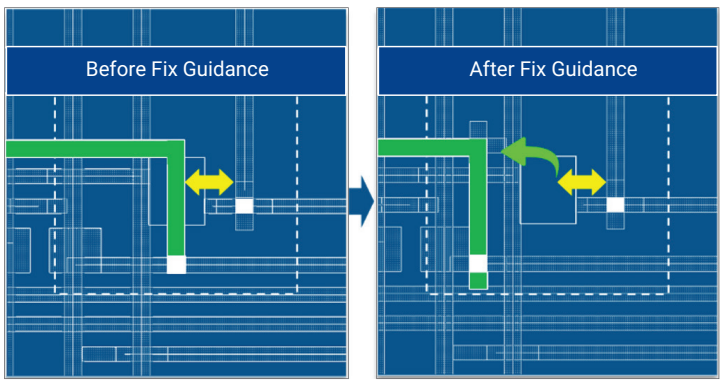

Figure 8: Router driven automatic DRC repair

IC Validator's seamless integration with Fusion Compiler and IC Compiler II enables an innovative layout auto-correction interface, which identifies DRC violations, including DPT decomposition violations and initiates automatic repairs. The corrections are applied by Fusion Compiler and IC Compiler II to alleviate DRC and DPT errors, and then validated with signoff foundry runsets using IC Validator Physical verification. Fusion integration makes it possible to maintain hotspot-free designs throughout implementation, further eliminating iterations.

Timing Aware Fill

At advanced nodes, fill insertion is mandatory to ensure manufacturability and high yield. But excessive fill can lead to build-up of coupling capacitance, impacting timing and resulting in unpredictable iterations with design. IC Validator enables single-pass fill implementation that is timing-aware to prevent such problems. Combined with IC Validator's fill-to-target technology, timing-aware fill efficiently balances timing and density and replaces multiple fill-analyze iterations with a single step. At advanced nodes, timing-awareness coupled with track-based fill enables higher fill densities along with greater control over fill density versus timing impact.

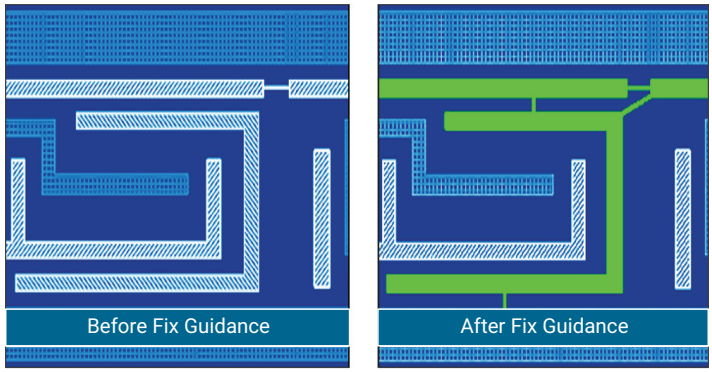

Figure 9: 3-color and 4-color patterning decomposition and auto stitching

Manufacturing at advanced node usually relies on Double Patterning Technology (DPT), which requires that a design be decomposable into two overlapping layout patterns. IC Validator offers comprehensive support for double patterning. IC Validator includes a native coloring (decomposition) engine based on flexible coding of DPT rules, and supports advanced capabilities such as stitching rules. With Fusion Technology, IC Validator provides signoff quality decomposition checking and automatic repair of DPT conflicts.

Comprehensive Physical Signoff Solution

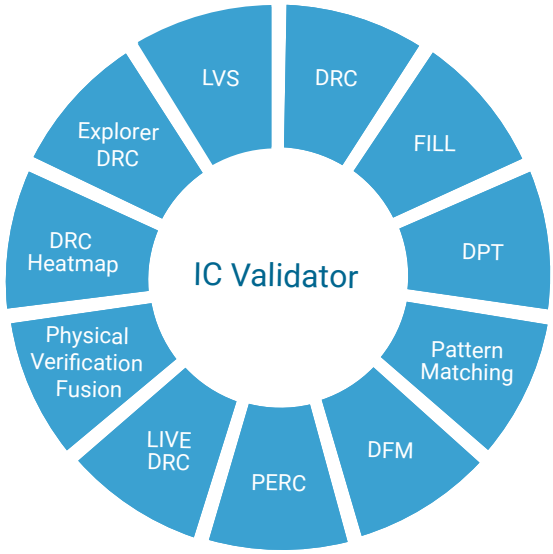

Figure 10: IC Validator comprehensive physical verification capabilities

Synopsys' IC Validator is the proven high performance and comprehensive signoff physical verification solution. Trusted by leading semiconductor companies and used in hundreds of production designs, IC Validator offers a physical verification tool suite including DRC, LVS, Programmable Electrical Rule Checks (PERC), dummy fill, and Design For Manufacturing (DFM) capabilities.

Foundry Qualification

Comprehensive foundry qualification is a necessary component of any successful physical verification solution. IC Validator is signoff certified by all major foundries. IC Validator is actively in production use for FinFETs, SOI and traditional technologies at established process nodes and advanced emerging process nodes by leading foundries.

Pattern Matching

IC Validator's pattern matching efficiently expands IC Validator's rule-based signoff engine for pattern-driven verification.This capability makes it possible to quickly identify and automatically correct manufacturability hotspots in a design by comparing against a library of known problematic layout patterns. IC Validator's patented pattern matching technology eliminates the need for convoluted rules, and with almost zero runtime penalty per pattern. IC Validator's pattern matching significantly reduces the time to achieve manufacturing compliance.

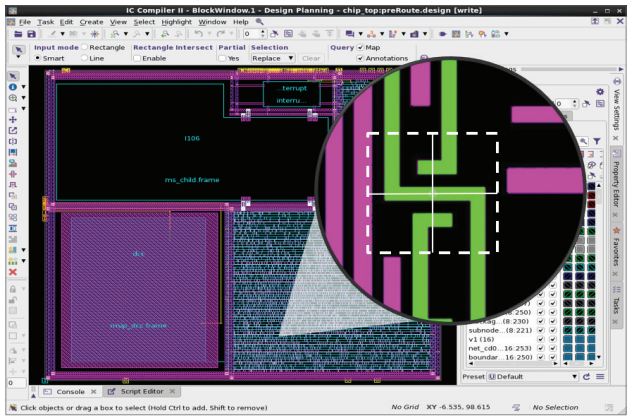

Figure 11: Pattern matching for ultra-fast manufacturing detection and prevention

Double, Triple, Quad Patterning

Manufacturing at 20nm and below usually relies on Double Patterning Technology (DPT), which requires that a design be decomposable into two overlapping layout patterns. IC Validator offers comprehensive support for double patterning. IC Validator includes a native coloring (decomposition) engine based on flexible coding of DPT rules and supports advanced capabilities such as stitching rules. With In-Design technology, IC Validator provides signoff quality decomposition checking and automatic repair of DPT conflicts.

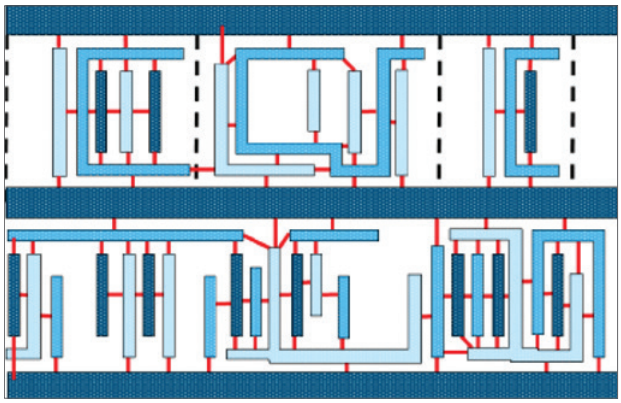

Figure 12: Signoff quality double, triple and quad patterning verification and correction

PERC

IC Validator PERC is a reliability verification solution that enables customized checking for EOS/ESD/ERC rules. Programmable Electrical Rule Checks (PERC) supports checking of Netlist Domain Checks (NDC), Mixed-Mode Checks (MMC), also Current Density (CD), and Point-to-Point Resistance (P2P). IC Validator PERC technology provides fast performance, scalability and intuitive debugging for reliability verification.

PERC leverages the hierarchical processing power of IC Validator to provide a unique chip level solution. Key capabilities include:

- Current density checking with StarRC extraction
- Point-to-point resistance checking with StarRC extraction
- Voltage based spacing checks
- All topology checks
- All layout checks

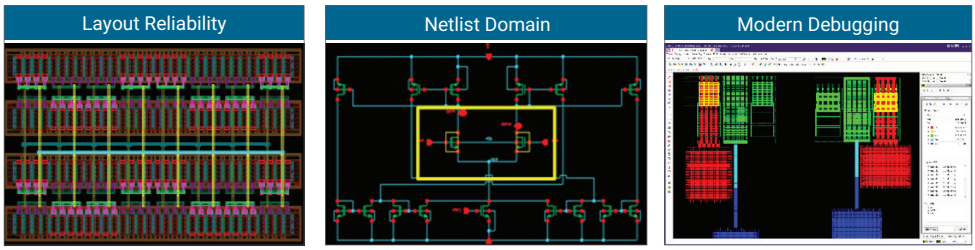

Figure 13: Comprehensive reliability verification with IC Validator PERC

Live DRC Checking

IC Validator Live DRC technology joins a signoff quality geometry engine, foundry signoff runsets and supported layout tools to enable signoff quality in-context viewport DRC checking. Foundry signoff runsets are initially cached once per user, then DRC checks will be immediately ran based upon the active viewport the designer choses. Custom layout designers can run DRC directly from the layout canvas to get immediate DRC feedback within seconds. This enables interactive design and verify flow and enhances designer productivity.

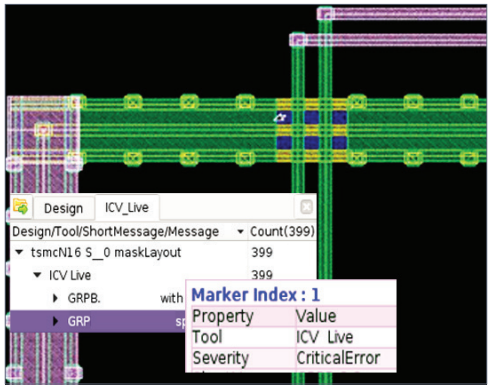

Figure 14: Live DRC checking for custom design flows

Full Custom Frameworks

IC Validator supports full interoperability for job execution, layout error shape probing, schematic cross probing with Visualization User Environment (VUE) within Synopsys Custom Compiler™ and supported third party solutions. IC Validator with StarRC for post layout extraction will write a logical extracted view to Openaccess. IC Validator LVS provides the ideal layout extracted netlist used by StarRC for the Custom Compiler integrated CustomSim-RA EM/IR reliability analysis flow.

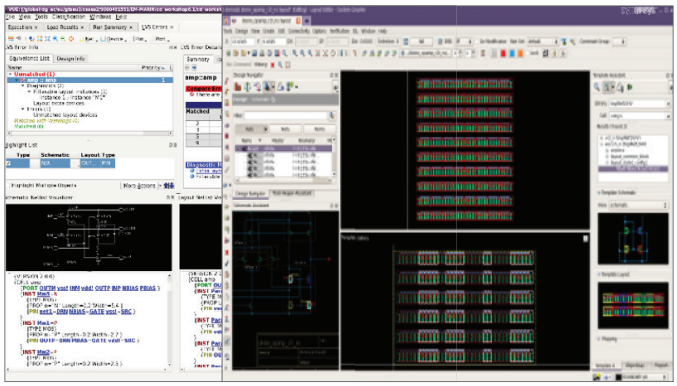

Figure 15: Execution and debug from with custom design tools

Layout Visualization: Integration with IC Workbench EV Plus

IC WorkBench EV Plus is a powerful, hierarchical layout visualization and analysis tool. It allows viewing, editing and merging of GDSII and OASIS layouts from small IP blocks to complex system on chips. The tool provides easy debugging of hierarchy and placement of cells and shapes.

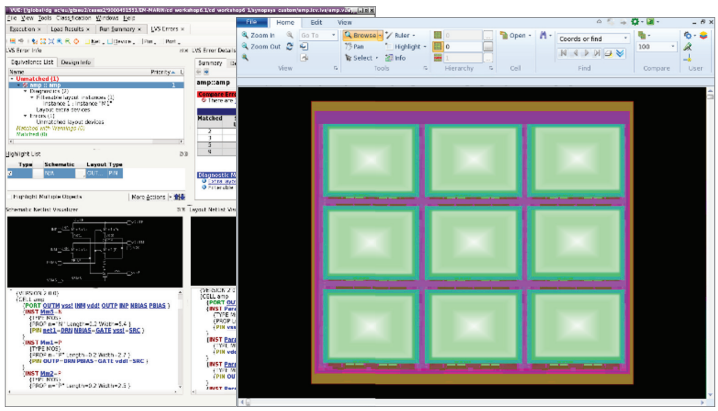

Figure 16: High-speed GDS-OASIS layout visualization